REMARKS

Claim 1 and 2 have been amended in order to more particularly point out, and distinctly claim the subject matter to which the applicants regard as their invention. Claim 9 has been cancelled. No new matter has bee added.

Claims 1-5 and 8-10 are pending in this application. Claims 6 and 7 are withdrawn. Claim 1-5 and 8-10 stand rejected.

Claim Rejections under 35 USC §102

Claims 1 and 8-9 are rejected under 35 U.S.C. §102(b) as being anticipated by Watanabe et al. (US 6,326,561).

The present invention includes three embodiments. In the first embodiment a wiring substrate (1) is shown having an interlayer insulating film (14) which is formed on the base substrate (10) and a first wiring pattern (12). Via holes (14a to 14d) are formed the interlayer insulating film (14) on the first wiring pattern (12) and via posts (11) is filed in the via holes (14a-14d). Further, a second wiring pattern (12a) is formed on the interlayer insulating film (14) and connected to the via post (11).

As indicated in paragraph 30 of the specification the via holes (14a to 14d) are arranged under the second wiring pattern (12a) which is just under connection pad P. These via holes (14a to 14d) are within a 200 μm of the connection pad P. In this way the via posts (11) in the via holes

(14a to 14d) function as struts so that the connection pads P can withstand pressure or ultrasonic vibration applied in the ultrasonic flip-chip packaging process.

Watanabe et al. describes a thin-film multilayer wiring board having a substrate (1) made with an insulating layer (2) formed thereon. In turn a metallic wiring layer (4) is formed on the contacting with the substrate (1) and via holes formed in the insulating layer (2). A number of insulating layers (2) are formed each having a metallic wiring layer (4) laminated thereon. The metallic wiring layers (4) are connected via studs (3) made of a conductive metal filled in the via holes.

The Examiner points out that in FIG. 10 of Watanabe, a wiring substrate similar to the wiring substrate of claim 1 is disclosed, and the via post 3 is arranged under a bump 3 of LSI 14 whose bump 3 is flip-chip packaged to a wiring pattern 4.

The Examiner argues that he phrase "by an ultrasonic flip chip packaging" is a process designation, thus the phrase can not be admitted as constitution of invention.

In Watanabe, it is not considered that to withstand pressure or ultrasonic vibration in case of ultrasonic flip-chip packaging at all, but, in FIG. 10, the via post 3 is arranged under the bump 16 of the LSI 14 unexpectedly.

Therefore, claim 1 patentably distinguishes over the prior art by reciting,

> "An electronic parts packaging structure comprising: a wiring substrate which has a structure in which a wiring pattern including a connection pad to which a bump of an electronic parts is bonded is provided on an insulating film, and the wiring substrate in which a via hole into which a via post is filled is arranged in a portion in the insulating film under the connection pad; and the electronic parts whose bump is ultrasonic flip-chip packaged to the connection pad; <u>wherein said via posts in said</u>

via holes are positioned at positions corresponding to said bumps of said electronic parts respectively, so that said via ports function as struts which can prevent that said connection pads eat into the insulating film by withstanding pressure or ultrasonic vibration, in case that electronic parts whose pumps are ultrasonic flip-chip packaged to said connection pads." (Emphasis Added)

Therefore, withdrawal of the rejection of claims 1 and 8-9 under 35 U.S.C. §102(b) as being anticipated by Watanabe et al. (US 6,326,561) is respectfully requested.

Claim Rejections under 35 USC §103

Claim 2 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Watanabe.

This rejection is similar to that supplied for claim 1 with the exception that asserts that it would be obvious to place the via holes within 200 μm of the connection pad for compact packaging. However, paragraph 30 of the specification states that,

"Since the via holes 14a to 14d are arranged under the second wiring pattern 12a just under the connection pad P or within a 200 μm from the connection pad P respectively, the via post 11 in the via holes 14a to 14d function as the strut so that the connection pads P can withstand the pressure or the ultrasonic vibration applied in the ultrasonic flip-chip packaging. As a result, it can be prevented upon the ultrasonic flip-chip packaging that the connection pads P are pressed into the interlayer insulating film 14 and are deformed."

Therefore, the purpose for 200 μm is so that the connection pads P can withstand the pressure or the ultrasonic vibration applied in the ultrasonic flip-chip packaging. Therefore claim 2 has been amended to reflect this feature. In Watanabe, since ultrasonic flip-chip packaging the LSI (14) is not considered at al, a diameter of the via post (3) is considerably thin compared with the bump (16) of

the LSI (14). Also, via post (3) whose position is shifted from a center portion of the bump (16) exists (Fig. 10). Accordlingly via posts (3) cannot function as struts in Watanabe.

Therefore, claim 2 patentably distinguishes over the prior art of record by reciting,

> "An electronic parts packaging structure comprising: a wiring substrate which has a structure in which a wiring pattern including a connection pad to which a bump of an electronic parts is bonded is provided on an insulating film, and the wiring substrate in which a via hole into which a via post is filled is arranged in a predetermined portion in the insulating film under the wiring pattern connected connection pad within 200 μm from the connection pad; and the electronic parts whose bump is ultrasonic flip-chip packaged to the connection pad,wherein said via posts in said via holes are positioned at positions within 200 μm from said connection pad concerning with said bumps of said electronic parts respectively, so that said via posts function as struts which can prevent that said connection pads eat into the insulating film by withstanding pressure or ultrasonic vibration, in case that electronic parts whose bumps are ultrasonic flip-chip packaged to the connection pad." (Emphasis Added)

Therefore, withdrawal of the rejection of claim 2 under 35 U.S.C. §103(a) as being unpatentable over Watanabe is respectfully requested.

Claims 3 and 5 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Watanabe in view of Umematsu et al. (U.S. 6,399,897).

Umematsu et al. describes a multi-layer wiring substrate includes both signal vias (58) and dummy vias (58a).

Claims 3 and 5 are allowable by reason of their dependence from allowable independent claims. Therefore, withdrawal of the rejection of claims 3 and 5 under 35 U.S.C. §103(a) as being unpatentable over Watanabe in view of Umematsu et al. (U.S. 6,399,897) is respectfully requested.

Claim 10 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Watanabe in view of Ohuchi (U.S. 6,590,287).

Ohuchi describes a packaging structure for a semiconductor device uses gold bumps.

Claim 10 is allowable by reason of its dependence from an allowable independent claim. Therefore, withdrawal of the rejection of claim 10 under 35 U.S.C. §103(a) as being unpatentable over Watanabe in view of Ohuchi (U.S. 6,590,287) is respectfully requested.

Conclusion

In view of the aforementioned amendments and accompanying remarks, claims 1-5, 8 and 10, as amended, are believed to be in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact the applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, the applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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